Fig. 1

(BACKGROUND)

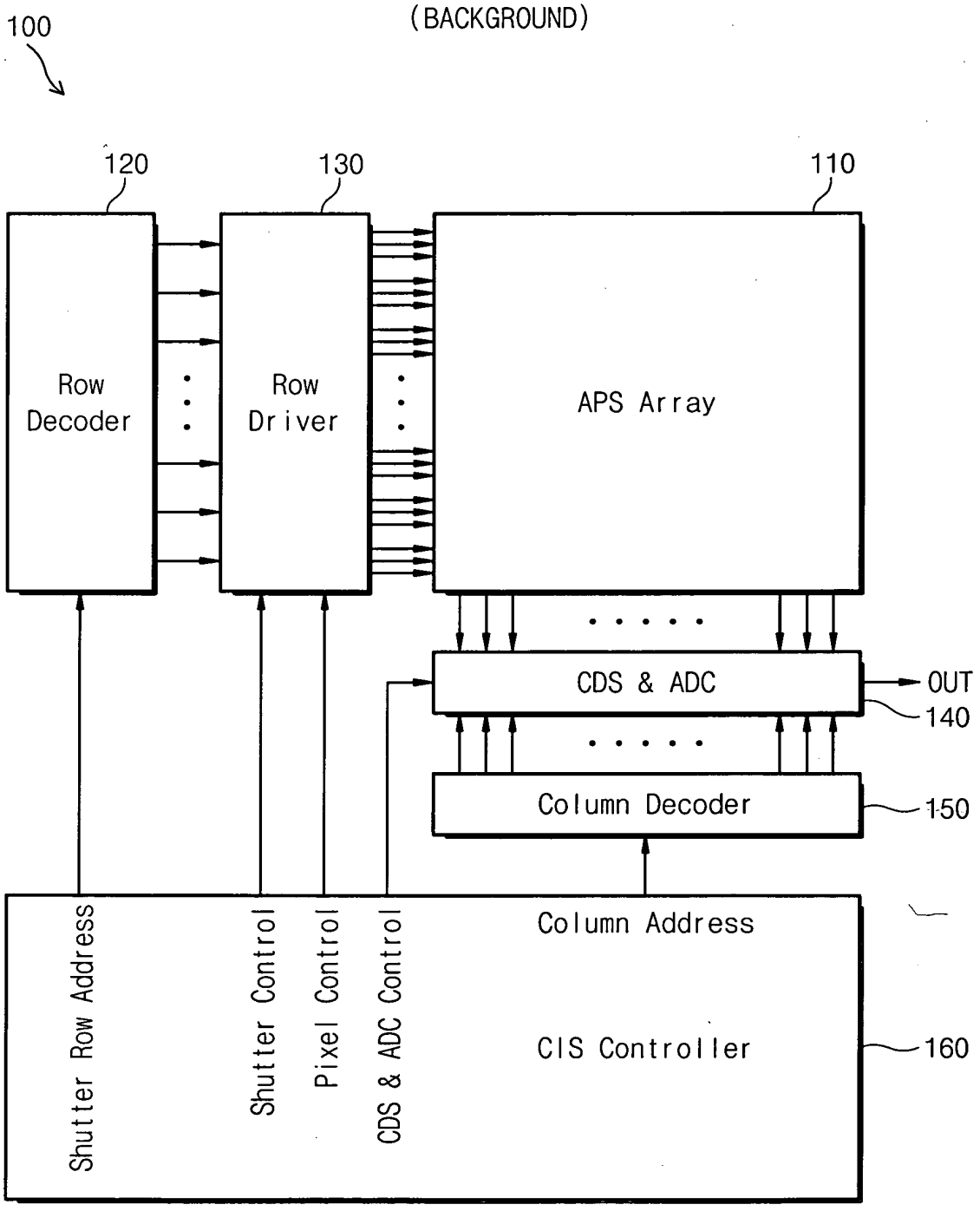


Fig. 2

(BACKGROUND)

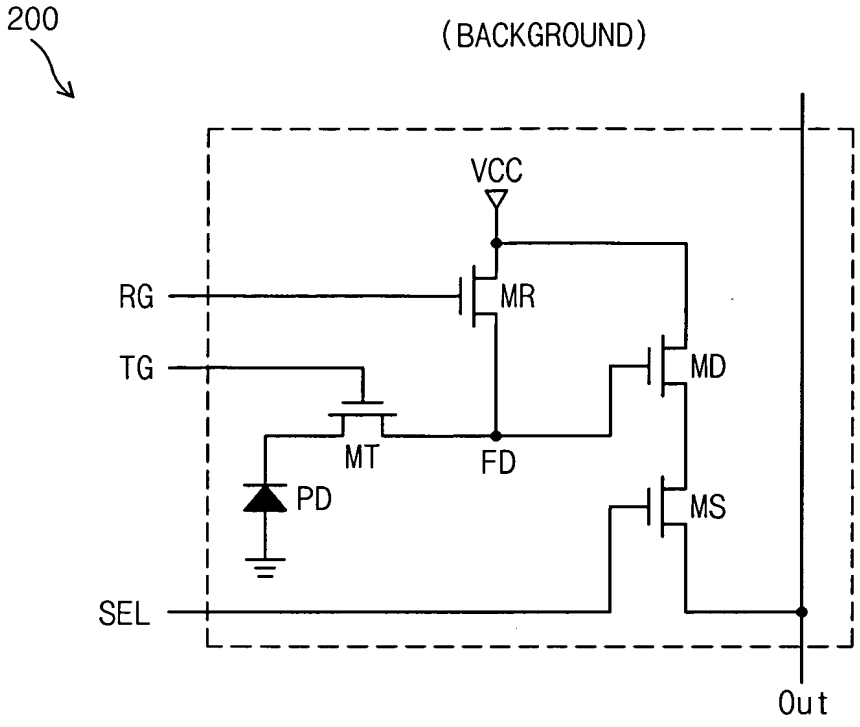


Fig. 3

(BACKGROUND)

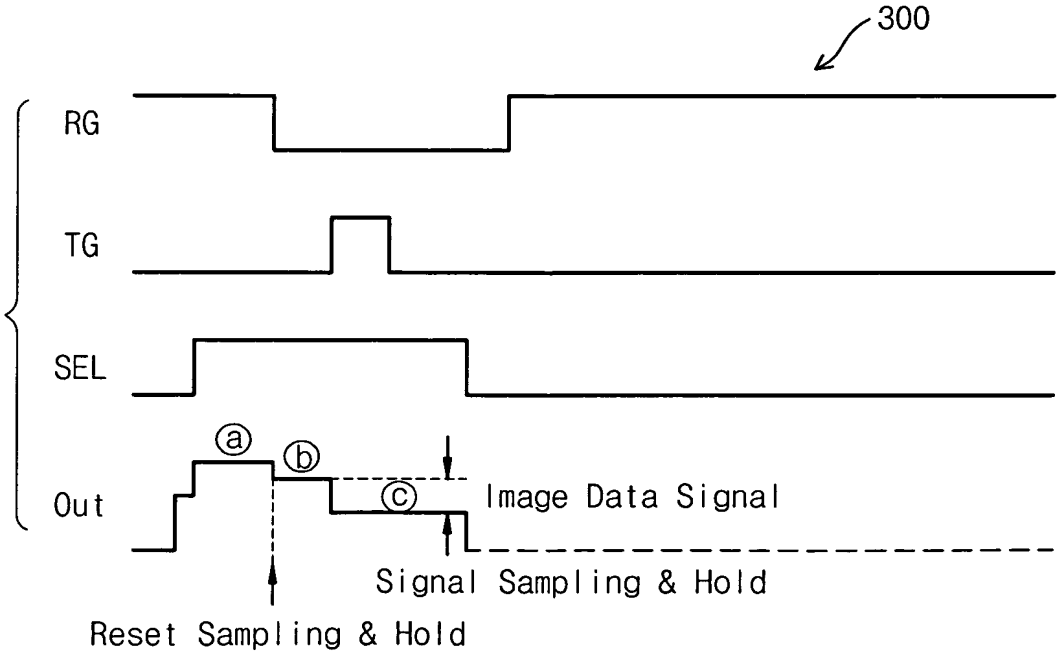


Image Data Signal = Reset Level - Signal Level

Fig. 4

(BACKGROUND)

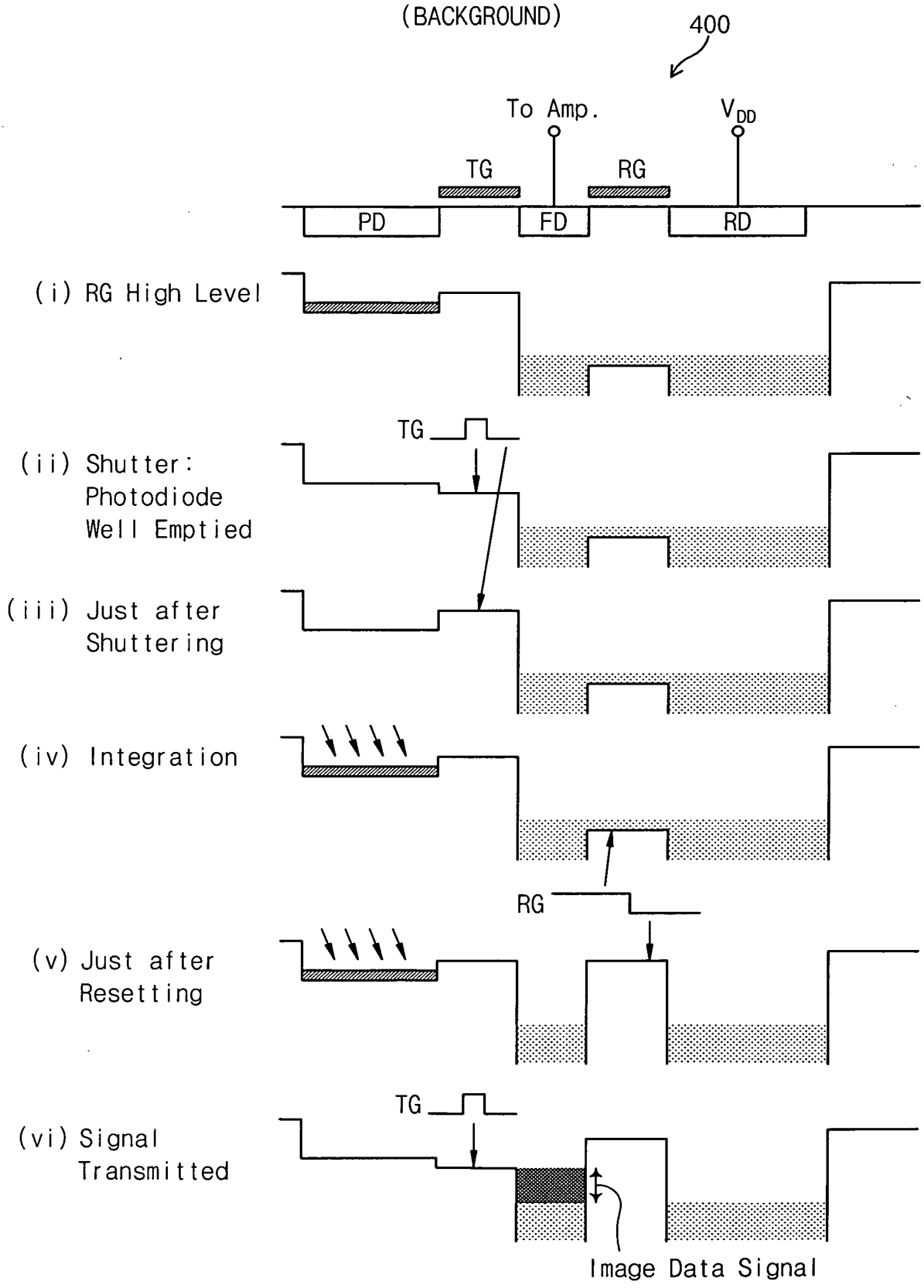


Fig. 5

(BACKGROUND)

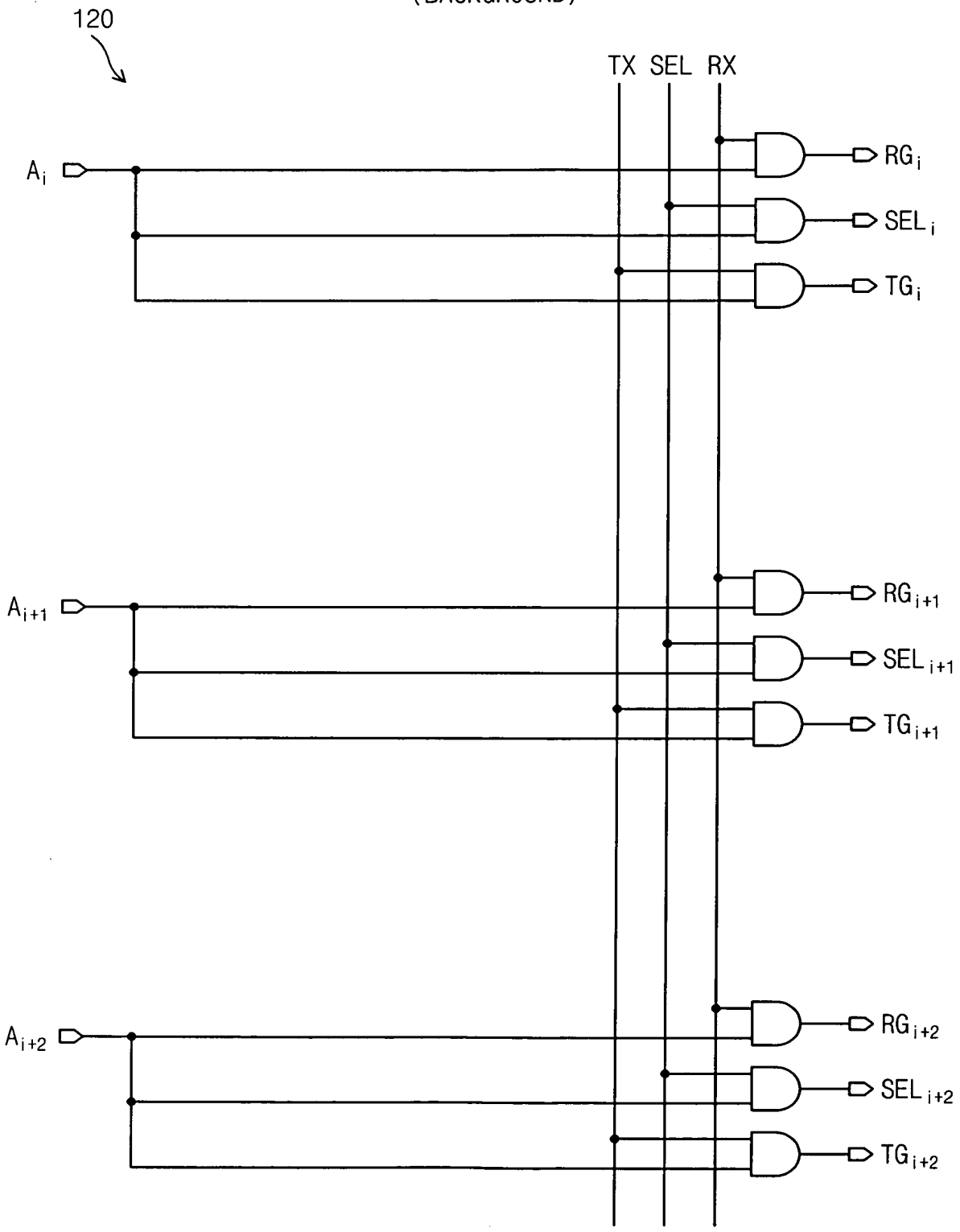


Fig. 6A

(BACKGROUND)

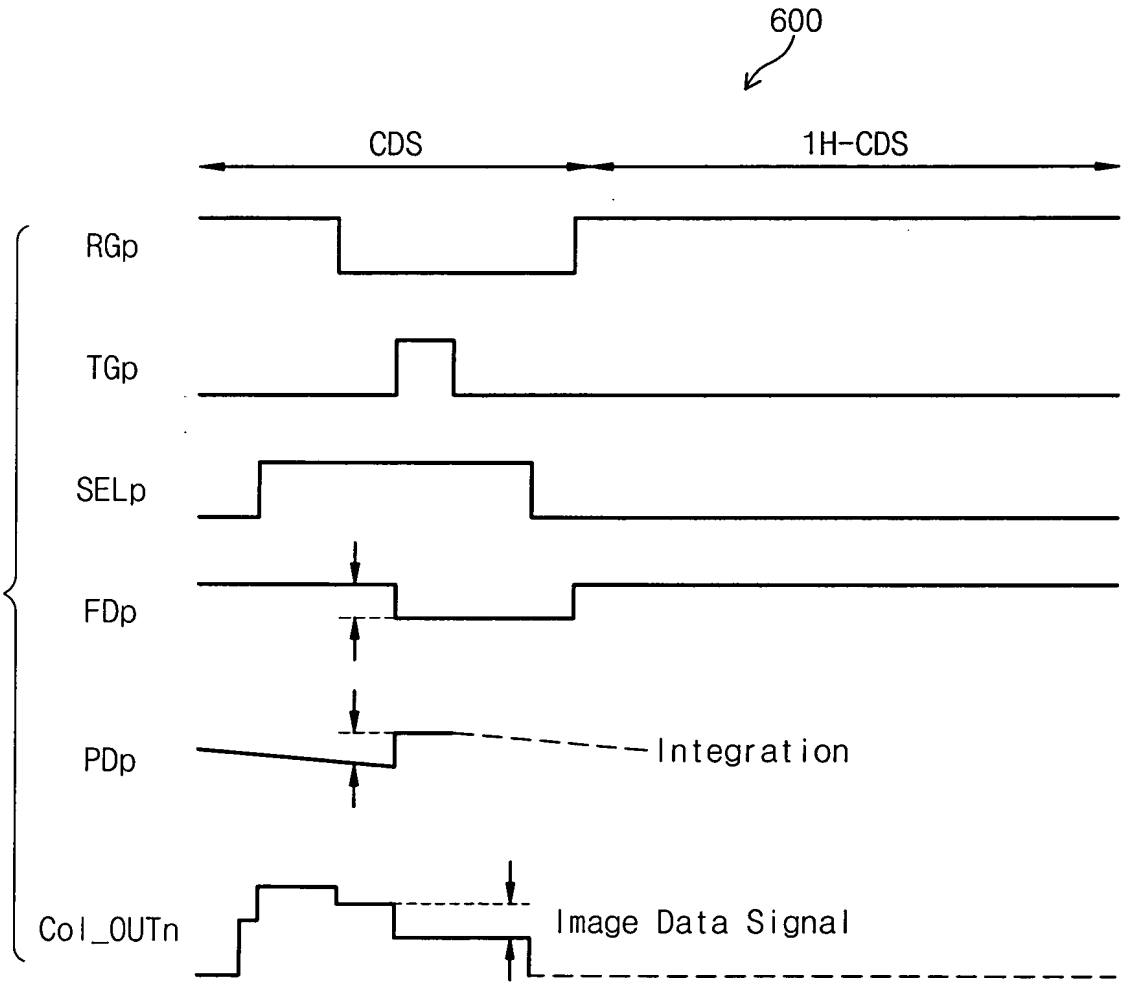


Fig. 6B

(BACKGROUND)

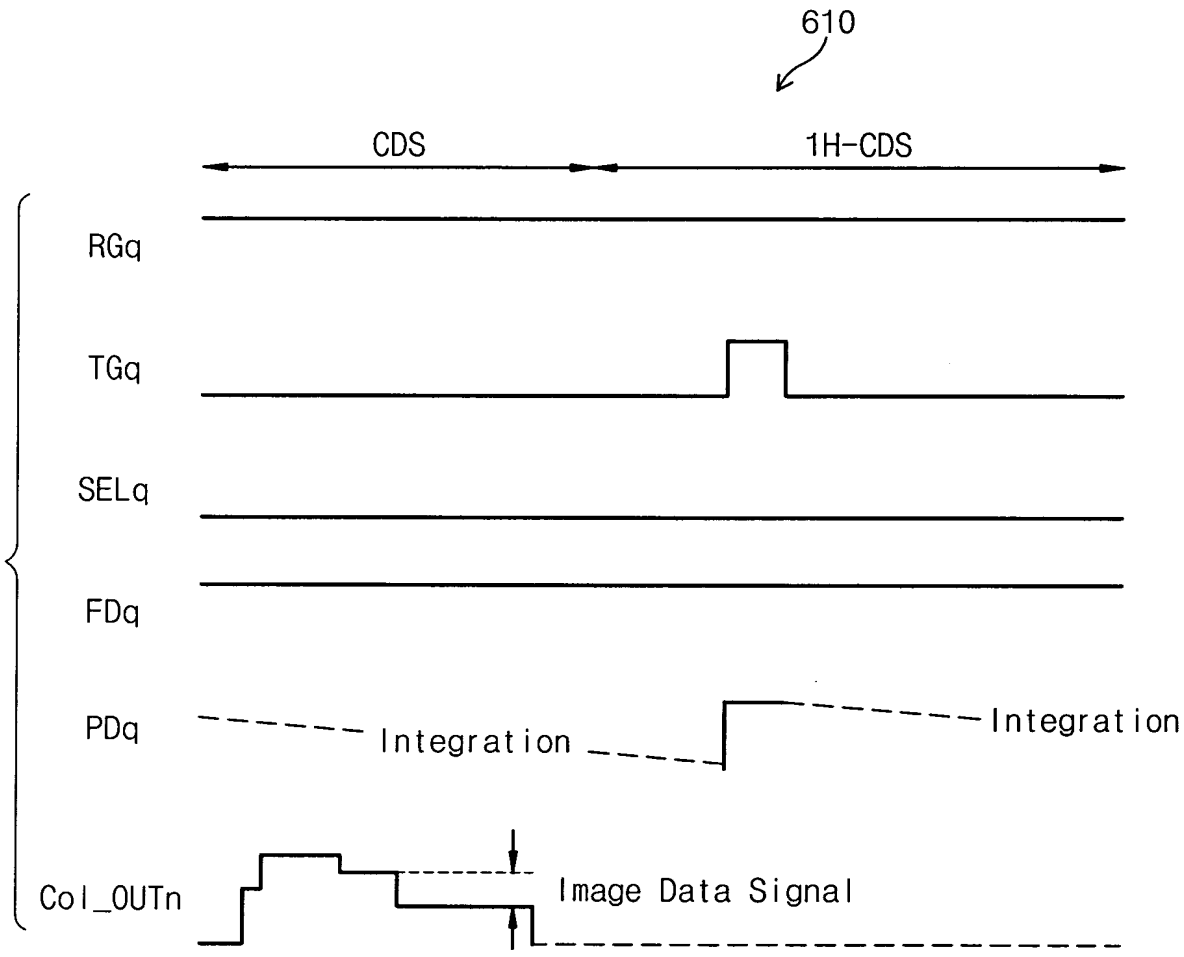


Fig. 7

(BACKGROUND)

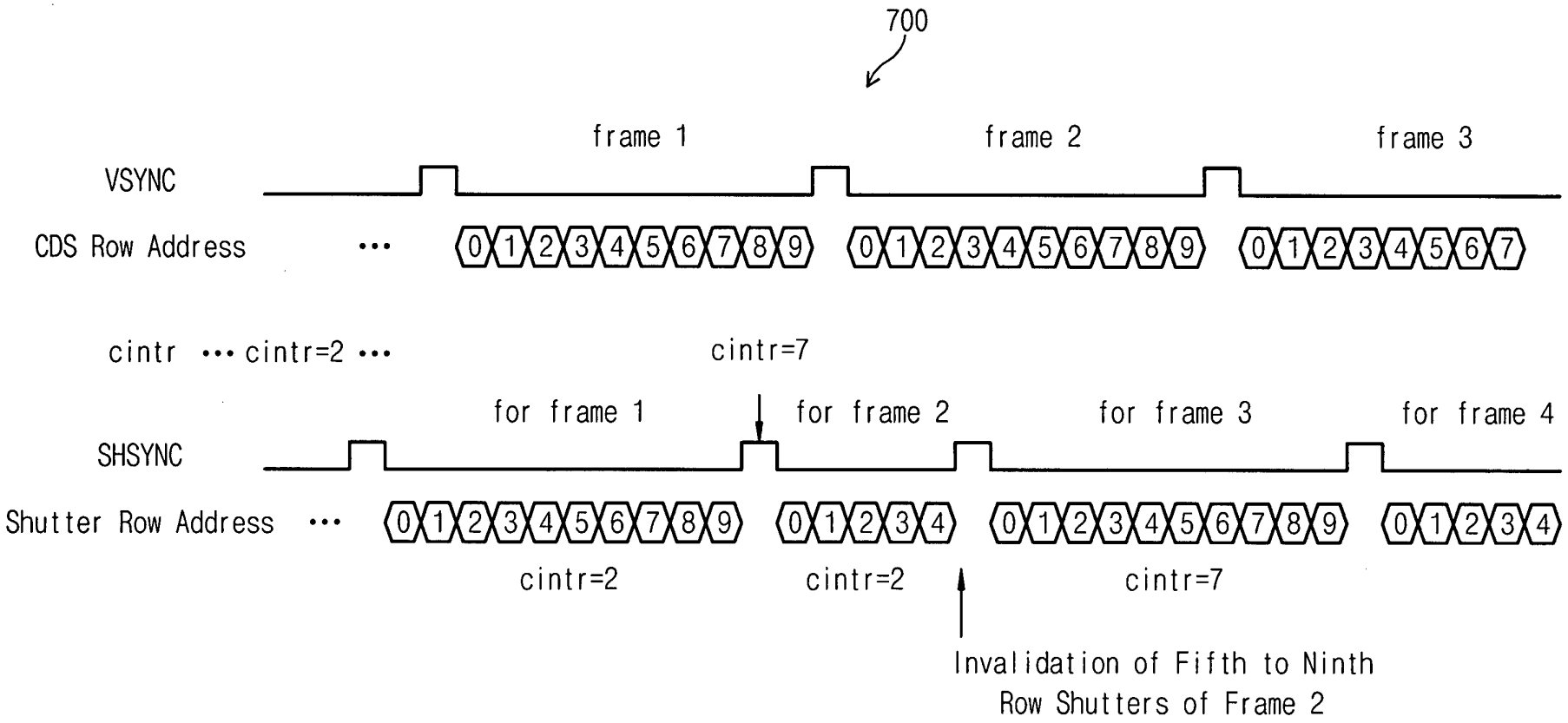


Fig. 8

(BACKGROUND)

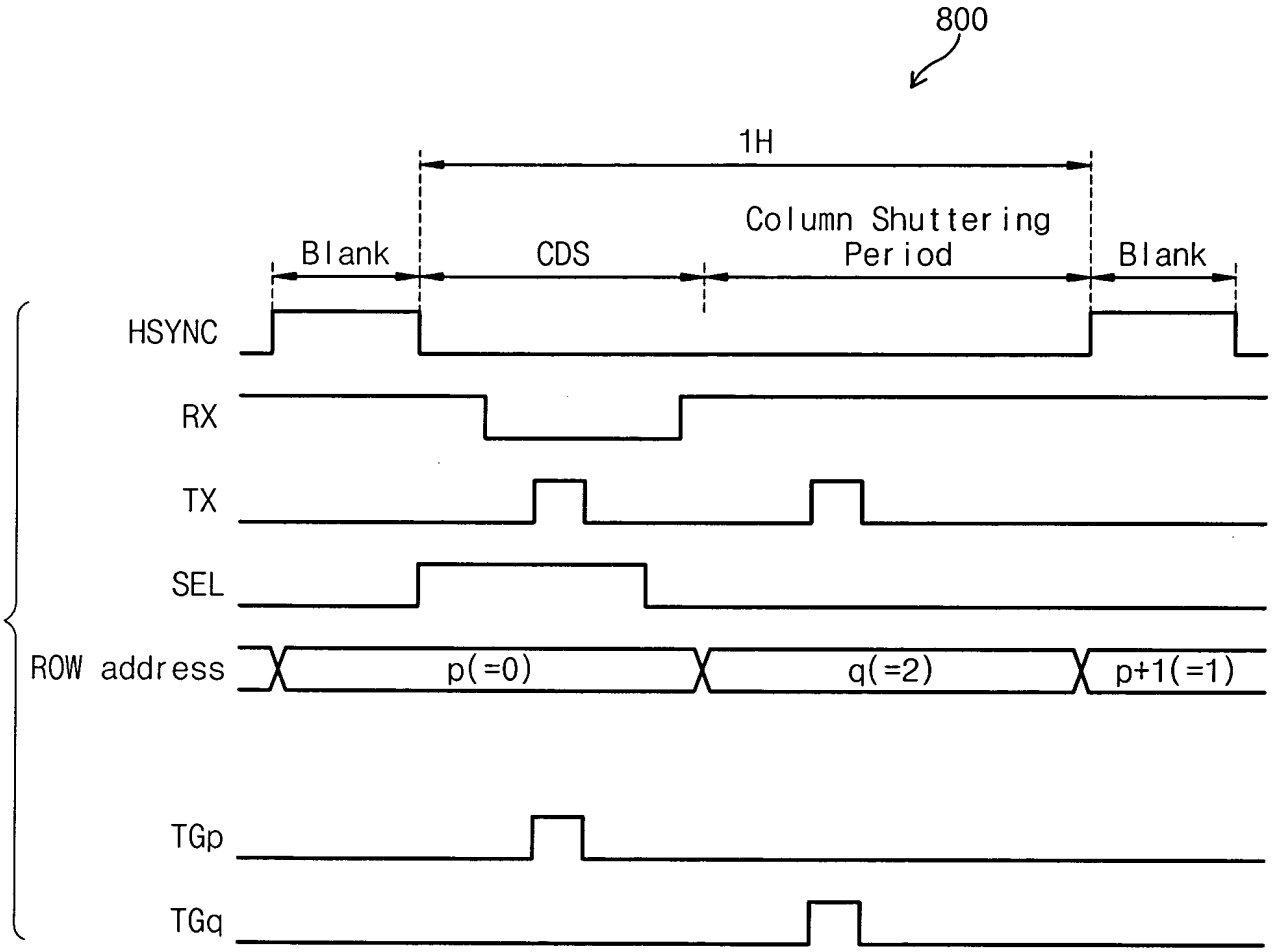


Fig. 9

(BACKGROUND)

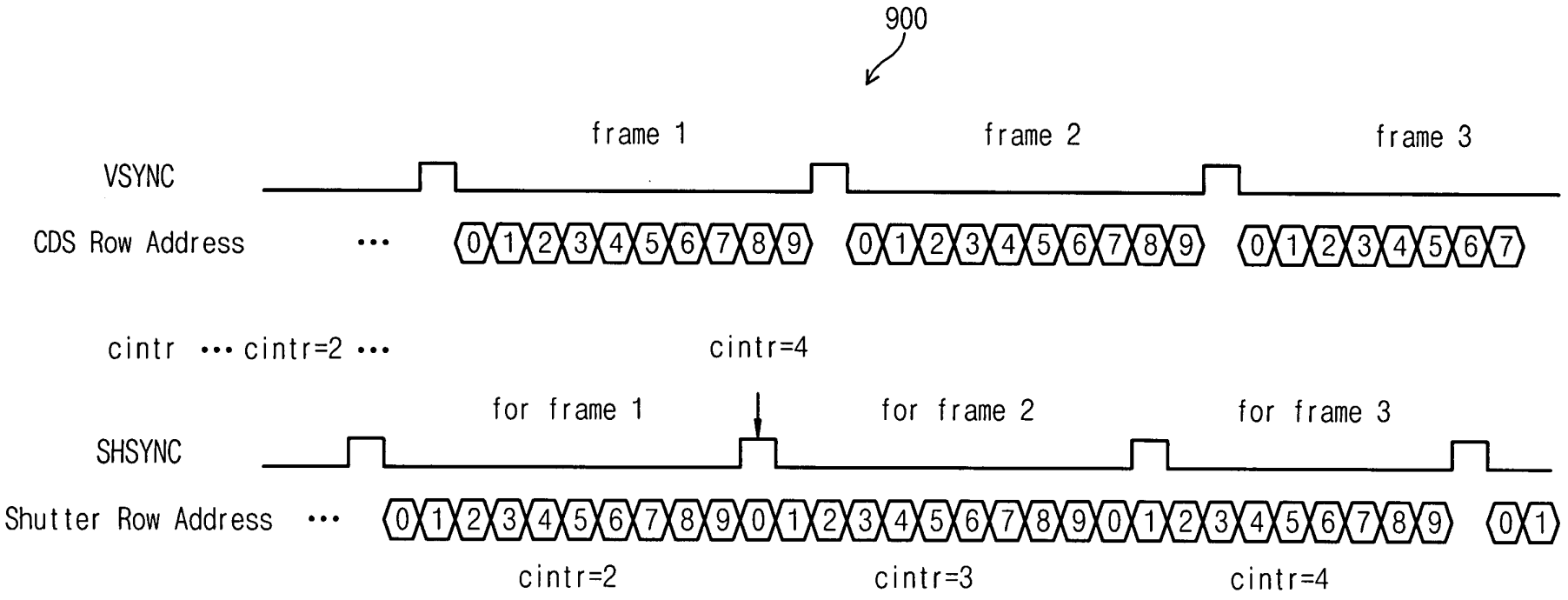


Fig. 10

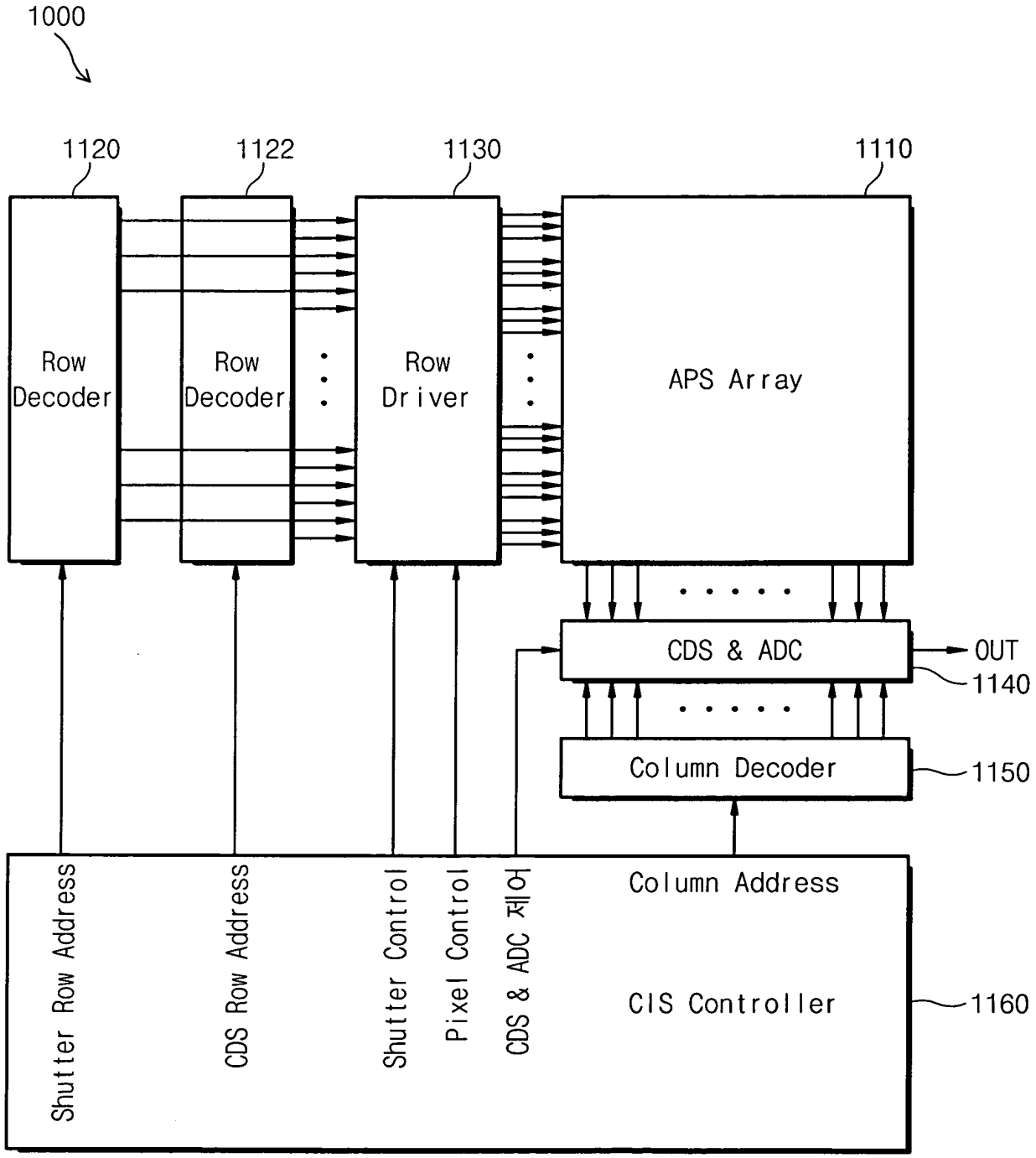

1000
1120
1122
1130
1110
Row Decoder
Row Decoder
Row Driver
APS Array
CDS & ADC
OUT
1140
Column Decoder
1150
Shutter Row Address
CDS Row Address
Shutter Control
Pixel Control
CDS & ADC 제어
Column Address
CIS Controller
1160

Fig. 11

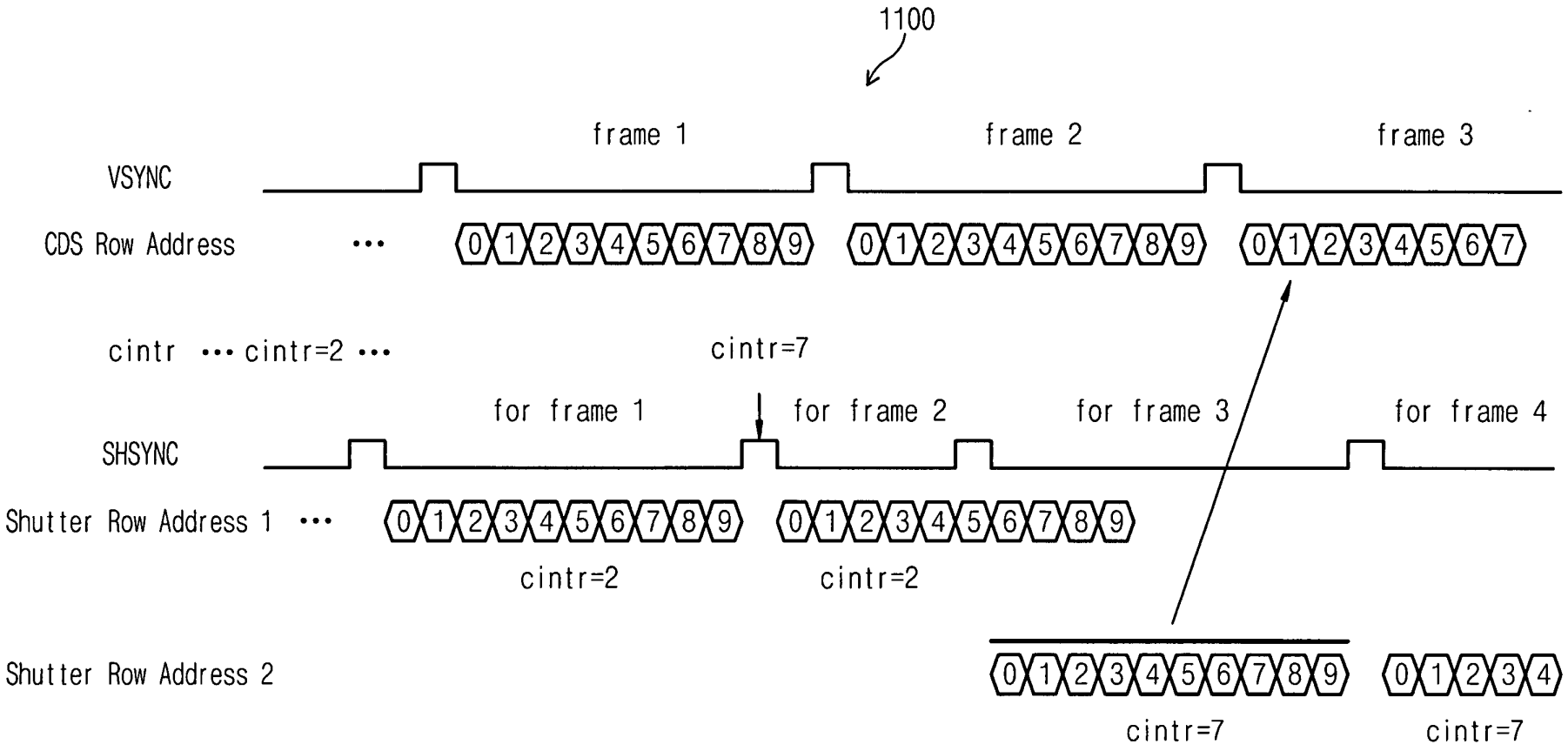

1100
frame 1
frame 2
frame 3
VSYNC
CDS Row Address
0 1 2 3 4 5 6 7 8 9
0 1 2 3 4 5 6 7 8 9
0 1 2 3 4 5 6 7
cintr ••• cintr=2 •••
cintr=7
for frame 1
for frame 2
for frame 3
for frame 4
SHSYNC
Shutter Row Address 1 •••
0 1 2 3 4 5 6 7 8 9
0 1 2 3 4 5 6 7 8 9
cintr=2
cintr=2
Shutter Row Address 2
0 1 2 3 4 5 6 7 8 9
0 1 2 3 4
cintr=7
cintr=7

Fig. 12

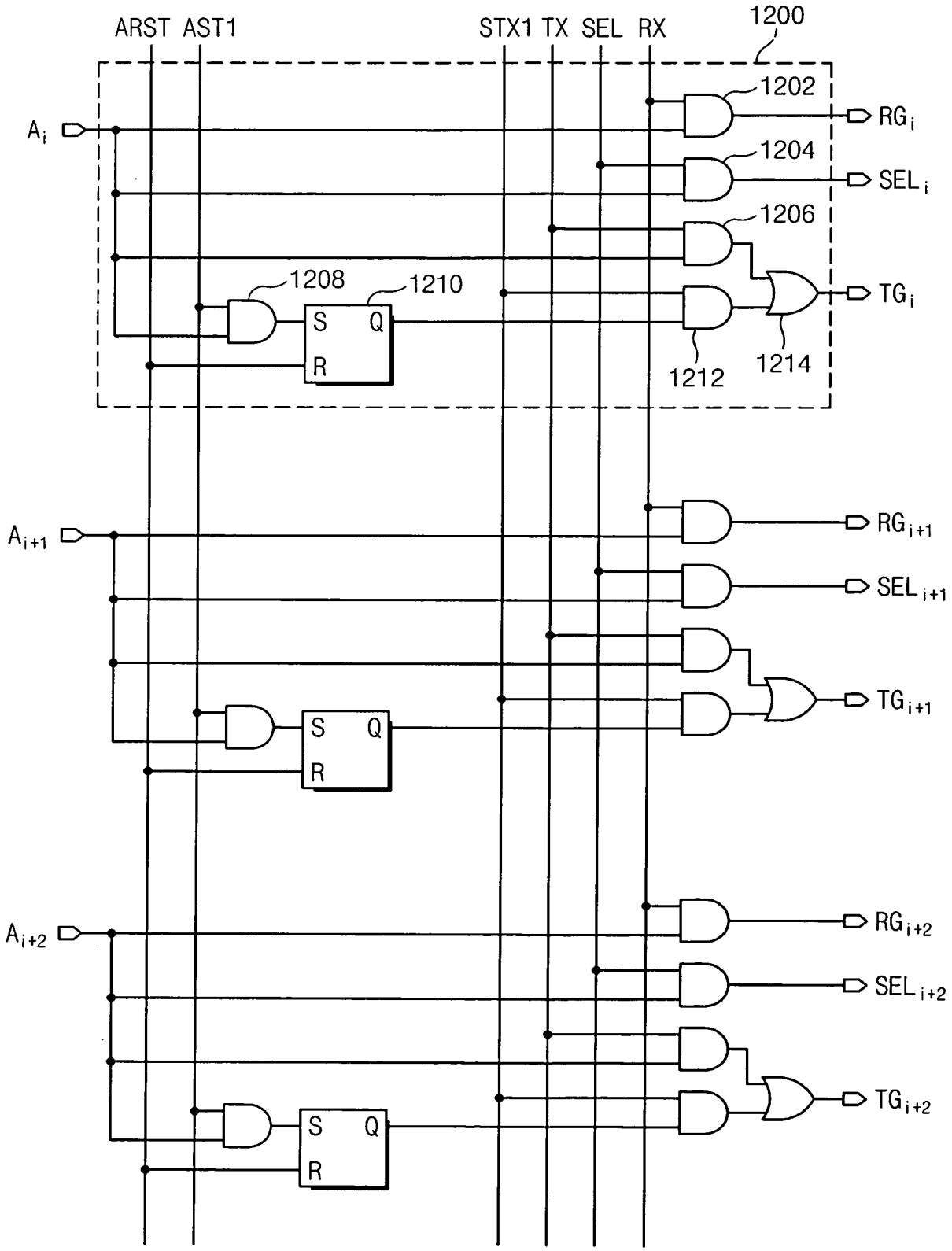

ARST
AST1
STX1
TX
SEL
RX
1200
1202
1204
1206
1208
1210
1212
1214
A_i
RG_i
SEL_i
TG_i
A_{i+1}
RG_{i+1}
SEL_{i+1}
TG_{i+1}
A_{i+2}
RG_{i+2}
SEL_{i+2}
TG_{i+2}
S
Q
R

Fig. 13

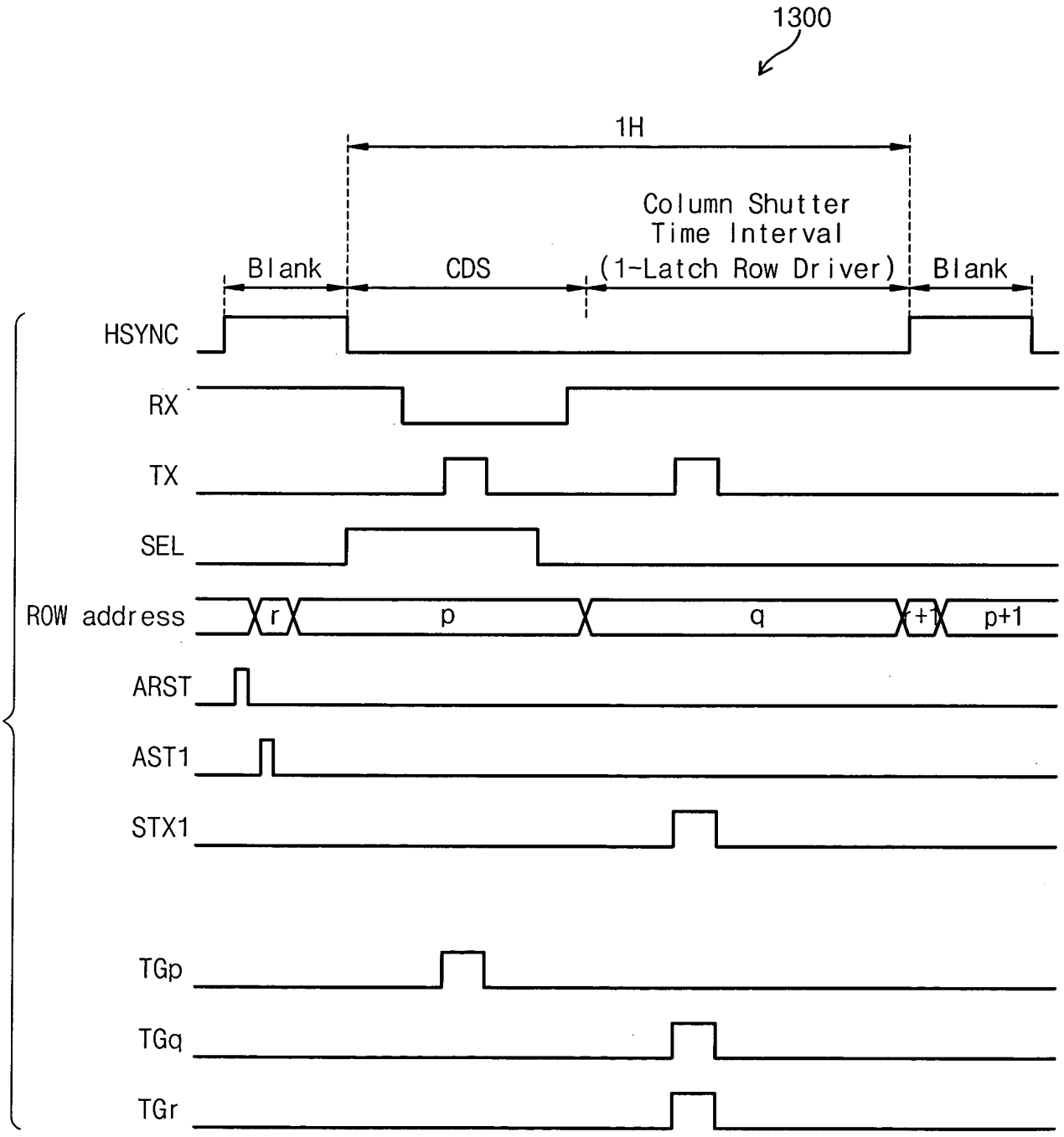

1300
1H
Column Shutter
Time Interval
(1-Latch Row Driver)
Blank
CDS
Blank
HSYNC
RX
TX
SEL
ROW address
r
p
q
r+1
p+1
ARST
AST1
STX1
TGp
TGq
TGr

Fig. 14

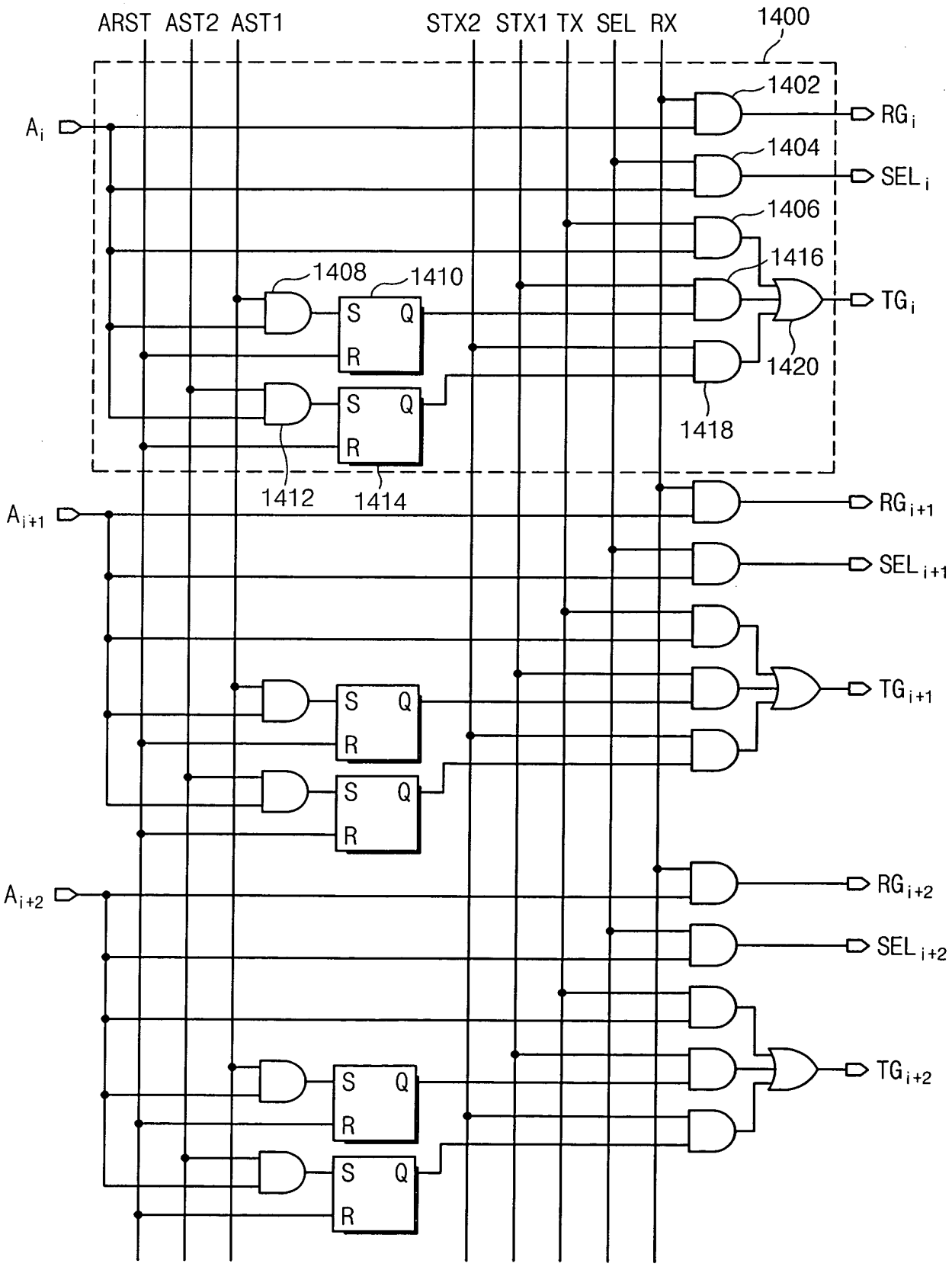
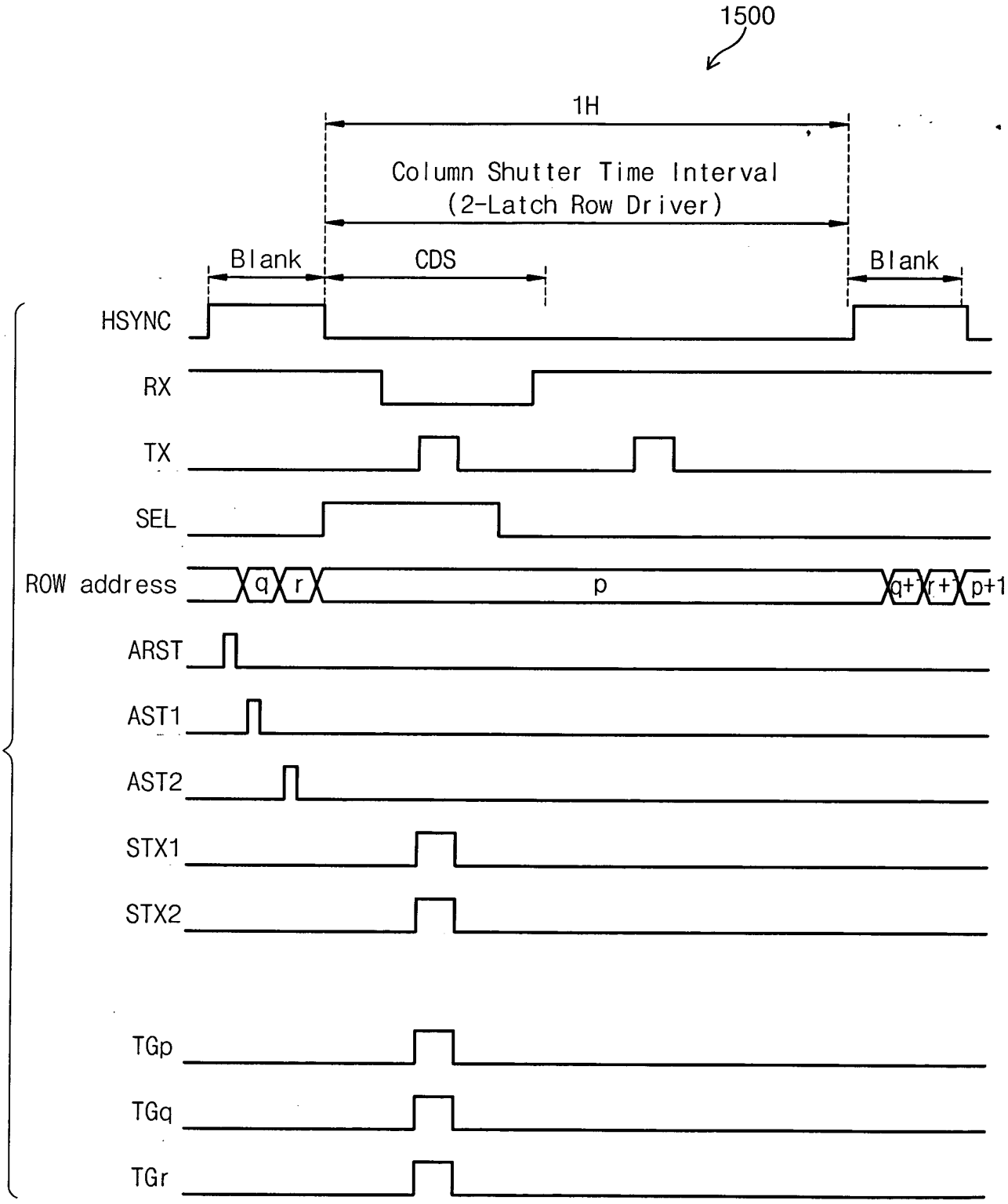

ARST
AST2
AST1
STX2
STX1
TX
SEL
RX
1400
1402
1404
1406
1408
1410
1412
1414
1416
1418
1420
A_i
A_i+1
A_i+2
RG_i
SEL_i
TG_i
RG_i+1
SEL_i+1
TG_i+1
RG_i+2
SEL_i+2
TG_i+2
S
Q
R

Fig. 15


1500
1H
Column Shutter Time Interval
(2-Latch Row Driver)
Blank
CDS
Blank
HSYNC
RX
TX
SEL
ROW address
q
r
p
q+1
r+1
p+1
ARST
AST1
AST2
STX1
STX2
TGp
TGq
TGr